Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A memory cell with at least two detectable states among which is an unprogrammed state, comprising:

a first branch in series between first and second terminals of application of a read voltage, the first branch including:

a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; and

a programming stage that includes a polysilicon first programming resistor having a terminal accessible by a first programming circuit capable of causing an irreversible decrease in a resistance value of the first programming resistor.

2. (Original) The memory cell of claim 1, wherein said decrease in the programming resistance value is predetermined and chosen to be greater than said first difference between the resistances of the pre-read stage.

3. (Original) The memory cell of claim 1, wherein the first programming circuit includes switches capable of applying a programming voltage greater than the read voltage across the first programming resistor.

4. (Original) The memory cell of claim 1, comprising at least one switch for isolating the pre-read stage with respect to the programming stage.

5. (Original) The memory cell of claim 1, wherein a reading of the cell state is performed in two successive steps during which said switchable resistors of the pre-read stage are alternately selected.

6. (Original) The memory cell of claim 5, wherein said terminal of the first programming resistor forms a read terminal of the cell capable of being connected to a first terminal of a read amplifier having a second terminal receiving at least one reference voltage chosen to be an intermediary level between the voltage level taken by the read terminal in the two read phases, while the first programming resistor is in an unprogrammed state.

7. (Original) The memory cell of claim 1, wherein the first branch includes a first transistor, the memory cell further comprising a second branch that includes a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; a programming stage that includes a polysilicon second programming resistor having a terminal accessible by a second programming circuit capable of causing the irreversible decrease in a resistance value of the second programmable resistor; and a second transistor assembled as a flip-flop with the first transistor, the first programming resistor being connected to the second terminal by the second transistor and the second programming resistor being connected to the second terminal by the first transistor.

8. (Original) The memory cell of claim 7, wherein the switchable resistors of the second branch are controllable at the same time as the switchable resistors of the first branch, so that the respective values of the resistors selected in each of the branches are inverted.

9. (Original) The memory cell of claim 7, wherein the irreversible decrease to be applied to the programming resistors is chosen to be greater than the sum of the difference between the pre-read resistances and of a third nominal value difference between the programming resistors in an unprogrammed state.

10. (Original) A method for reading a memory cell with at least two detectable states among which is an unprogrammed state, the memory cell including a first branch in series between first and second terminals of application of a read voltage, the first branch including: a pre-read stage comprising, in parallel, two switchable resistors having different values with a predetermined first difference; and a programming stage that includes a polysilicon first programming resistor having a terminal accessible by a first programming circuit capable of causing an irreversible decrease in a resistance value of the first programming resistor, the method comprising performing two successive read steps during which said switchable resistors of the pre-read stage are respectively selected.

11. –23. (Canceled)

24. (New) The method of claim 10 wherein:

the first read step includes driving the first programming resistor with a first current from a first one of the switchable resistors and measuring a first electrical quantity at the first programming resistor;

the second read step includes driving the first programming resistor with a second current from a second one of the switchable resistors and measuring a second electrical quantity at the first programming resistor, the method further comprising:

detecting whether a memory state of the memory cell is a first memory state or a second memory state by comparing the first electrical quantity with the second electrical quantity.

25. (New) The method of claim 24 wherein the detecting step includes:

detecting the first memory state by detecting that the first electrical quantity logically equals the second electrical quantity; and

detecting the second memory state by detecting that the first electrical quantity does not logically equal the second electrical quantity.

26. (New) The method of claim 25 wherein detecting the first memory state includes detecting that the first and second electrical quantities are logical high values, the method further comprising detecting a third memory state by detecting that the first and second electrical quantities are logical low values.

27. (New) The method of claim 24 wherein the detecting step includes:

detecting the first memory state by detecting that the first electrical quantity is greater than the second electrical quantity; and

detecting the second memory state by detecting that the first electrical quantity is less than the second electrical quantity.

28. (New) The method of claim 10, wherein the memory cell further includes a second branch that includes a pre-read stage including, in parallel, two switchable resistors having different values with the first difference; and a programming stage that includes a second programming resistor having a terminal accessible by a second programming circuit capable of causing an irreversible decrease in a resistance value of the second programmable resistor, the method further comprising performing two successive read steps during which the switchable resistors of the pre-read stage of the second branch are respectively selected.

29. (New) The method of claim 28, wherein the switchable resistors of the second branch are controllable at the same time as the switchable resistors of the first branch, so that the respective values of the resistors selected in each of the branches are inverted.

30. (New) A memory device, comprising:

a memory cell with at least two detectable states among which is an unprogrammed state, the memory cell including:

a first branch in series between first and second terminals of application of a read voltage, the first branch including:

a pre-read stage including, in parallel, two switchable resistors having different values with a first difference; and

a programming stage that includes a first programming resistor having a terminal accessible by a first programming circuit structured to cause an irreversible decrease in a resistance value of the first programming resistor.

31. (New) The memory device of claim 30, wherein said decrease in the programming resistance value is predetermined and chosen to be greater than said first difference between the resistances of the pre-read stage.

32. (New) The memory device of claim 30, wherein the first programming circuit includes switches capable of applying a programming voltage greater than the read voltage across the first programming resistor.

33. (New) The memory device of claim 30, comprising a switch for isolating the pre-read stage with respect to the programming stage.

34. (New) The memory device of claim 30, wherein a reading of the cell state is performed in two successive steps during which said switchable resistors of the pre-read stage are alternately selected.

35. (New) The memory device of claim 34, wherein said terminal of the first programming resistor forms a read terminal of the cell and is connected to a first terminal of a read amplifier having a second terminal receiving at least one reference voltage chosen to be an intermediary level between the voltage level taken by the read terminal in the two read phases, while the first programming resistor is in an unprogrammed state.

36. (New) The memory device of claim 30, wherein the first branch includes a first transistor, the memory cell further comprising a second branch that includes a pre-read stage

comprising, in parallel, two switchable resistors having different values with a predetermined first difference; a programming stage that includes a polysilicon second programming resistor having a terminal accessible by a second programming circuit capable of causing the irreversible decrease in a resistance value of the second programmable resistor; and a second transistor assembled as a flip-flop with the first transistor, the first programming resistor being connected to the second terminal by the second transistor and the second programming resistor being connected to the second terminal by the first transistor.

37. (New) The memory device of claim 36, wherein the first branch includes first and second switches coupled respectively to first and second resistors of the switchable resistors of the first branch and the second branch includes third and fourth switches coupled respectively to third and fourth resistors of the switchable resistors of the second branch, wherein the first and fourth resistors have substantially identical resistance values, the second and third resistors have substantially identical resistance values, the first and third switches have respective control terminals coupled to one another and controlled by a first control signal, and the second and fourth switches have respective control terminals coupled to one another and controlled by a second control signal.

38. (New) The memory device of claim 36, wherein the irreversible decrease to be applied to the programming resistors is chosen to be greater than the sum of the difference between the pre-read resistances and of a third nominal value difference between the programming resistors in an unprogrammed state.